

# HIGH-Q MULTILAYER CERAMIC CHIP CAPACITORS



## FEATURES

Capacitance ranging from 0.1pF to 0.1μF  
 Voltage ratings of 25V~3600V  
 Size 0402 to 4040  
 Operating temperature rang of -55°C to +125°C  
 Lead-free termination,RoHS Compliant

## » APPLICATIONS

Applications include RF power amplifiers, low noise amplifiers.

## » ORDERING INFORMATION

CC41AC	0805	101	J	251	N	T
Series	Size code	Capacitance	Capacitance tolerance	Rated voltage	Termination finish	Packaging
CC41AC	0402 1210 0505 1111 0603 2225 0805 4040 1206	First two digits represent significant figures.Third digit specifies number of zeros.	B=±0.1pF C=±0.25pF D=±0.5pF F=±1% G=±2% J=±5%	First two digits represent significant figures.Third digit specifies number of zeros.	N=100%Sn	Packaging code

## » DIMENSIONS

Appearance	Case Size	Unit:mm								
		0402	0505	0603	0805	1206	1210	1111	2225	4040
	L	1.00 ± 0.15	1.40 ± 0.40	1.60 ± 0.25	2.00 ± 0.30	3.18 ± 0.25	3.18 ± 0.25	2.80 ± 0.50	5.70 ± 0.80	10.50 ± 0.70
	W	0.50 ± 0.15	1.40 ± 0.40	0.80 ± 0.25	1.25 ± 0.30	1.58 ± 0.25	2.41 ± 0.25	2.80 ± 0.50	6.35 ± 0.80	9.50 ± 0.50
	Tmax	0.61	1.45	1.00	1.40	1.27	1.52	2.60	4.50	4.50
	t	0.25 ± 0.15	0.40 ± 0.30	0.40 ± 0.25	0.50 ± 0.35	0.50 ± 0.25	0.50 ± 0.25	0.45 ± 0.30	0.80 ± 0.60	0.80 ± 0.60

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## » ELECTRICAL CHARACTERISTICS

No.	Dissipation Factor	Dielectric Strength	Insulation Resistance (25°C)	Q or Dissipation Factor C≥3pF	ESR C≥3pF	Temperature characteristic
CC41AC	$\text{tg } \delta \leq 10 \times 10^{-4}$	$U_R \leq 100V \quad 2.5U_R$ $100V < U_R \leq 200V \quad 1.5U_R + 100V$ $200V < U_R \leq 500V \quad 1.3U_R + 100V$ $U_R > 500V \quad 1.3U_R$	$IR \geq 10^9 M\Omega$	0402 $Q \times f \times C \geq 400$ 0505 $Q \times f \times C \geq 500$ 0603 $Q \times f \times C \geq 600$ 0805, 1206, 1210 & 1111 $Q \times f \times C \geq 800$ 2225 $Q \times f \times C \geq 1000$	0402 $ESR \leq 0.40\Omega$ 0505, 0603 $ESR \leq 0.35\Omega$ 0805 $ESR \leq 0.30\Omega$ 1206, 1210, 1111, 2225 $ESR \leq 0.25\Omega$	-55°C~125°C

# HIGH-Q MULTILAYER CERAMIC CHIP CAPACITORS

## » CAPACITANCE AND RATED VOLTAGE RANGE

CC41AC ((0±30)ppm/K)

Case size	0402		0505		0603 0805		1206			1111				1210			2225					4040							
Rated voltage(V)	25	50	150	250	250	250	100	200	500	50	100	200	500	100	200	500	300	500	1200	1500	2500	200	500	1000	1600	2500	3600		
0R1																													
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430																													
470																													
510																													
560																													
620																													
680																													
750																													
820																													

# HIGH-Q MULTILAYER CERAMIC CHIP CAPACITORS

## » CAPACITANCE AND RATED VOLTAGE RANGE

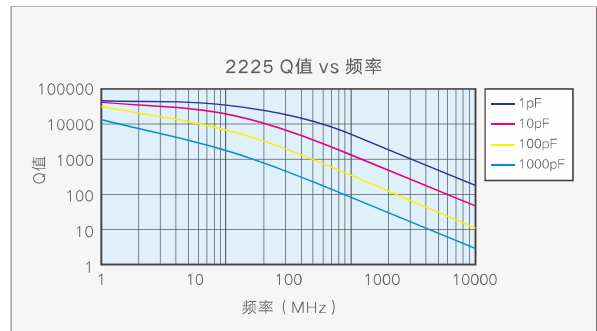
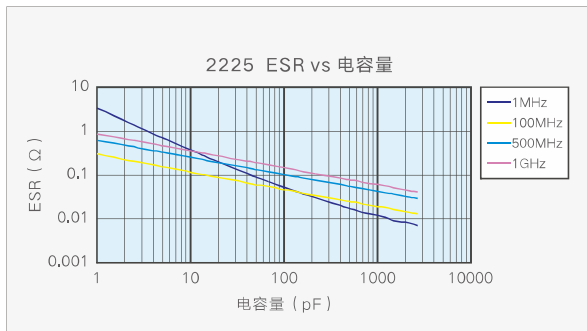
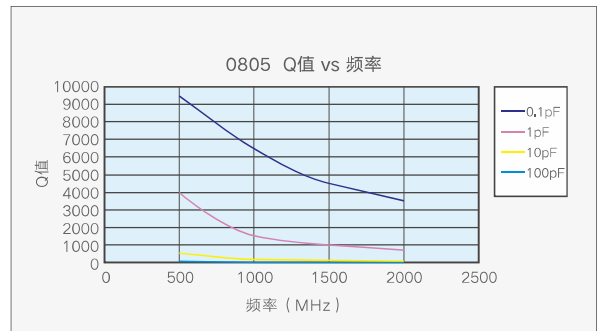
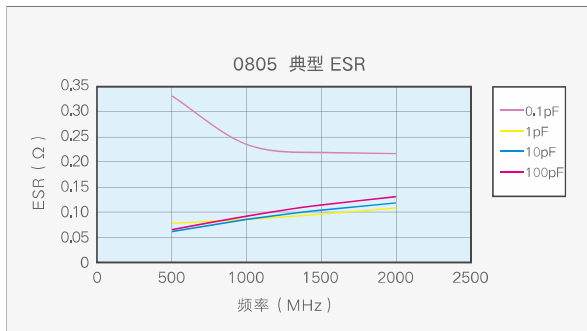
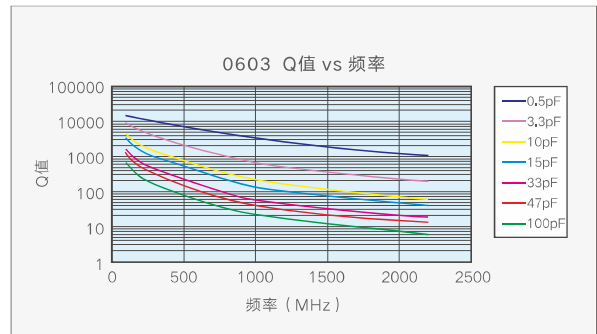
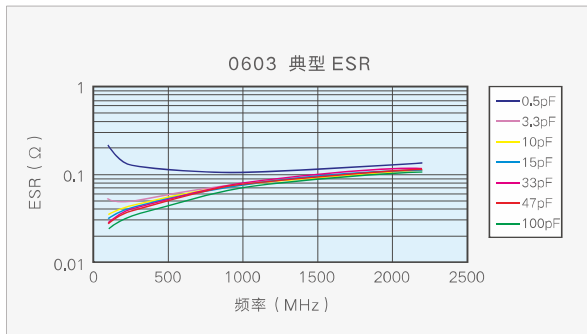
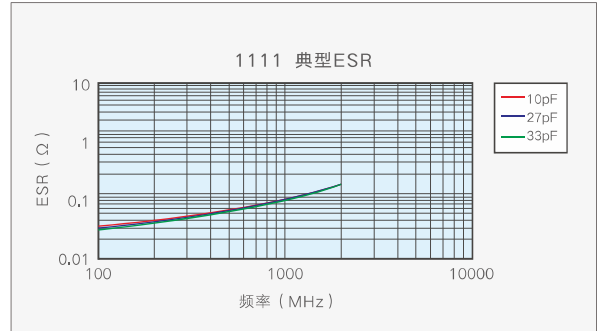
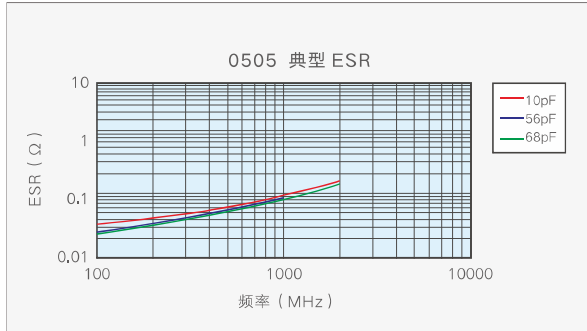
CC41AC ((0±30)ppm/K)

Case size	0402		0505		0603	0805		1206			1111				1210			2225					4040					
Rated voltage(V)	25	50	150	250	250	250	100	200	500	50	100	200	500	100	200	500	300	500	1200	1500	2500	200	500	1000	1600	2500	3600	
910																												
101																												
111																												
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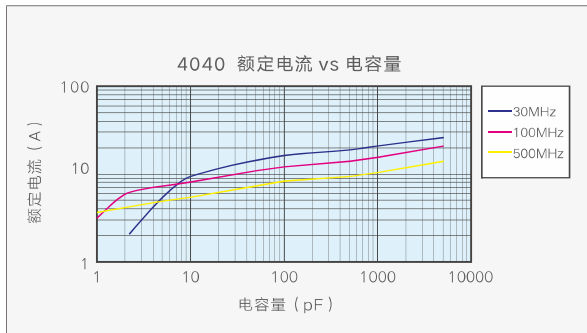
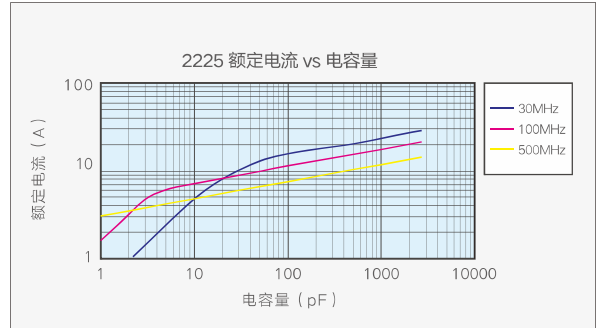
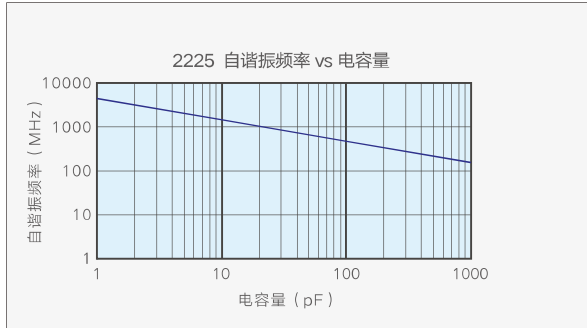
## » CHARACTERISTIC

CC41AC ( $0 \pm 30$ )ppm/K



# HIGH-Q MULTILAYER CERAMIC CHIP CAPACITORS

## » CHARACTERISTIC



# APPLICATION GUIDE FOR MULTILAYER CERAMIC CAPACITORS

## »» STORAGE

To maintain the solderability of terminal electrodes and to keep packaging materials in good condition, care must be taken to control temperature and humidity.

- Recommended conditions

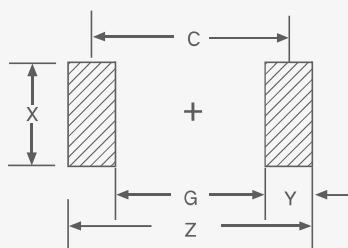
Temperature : Below 40°C , Humidity : Below 70% RH

Even under ideal storage conditions, solderability of capacitor is deteriorated as time passes, so capacitors shall be used within 12 months from the time of delivery. If exceeding the above period, please check solderability before using the capacitors.

## »» HEAT TREATMENT

The capacitance values of high dielectric constant capacitors will gradually decrease with the passage of time, so care shall be taken to design circuits. Even if capacitance value decreases as time passes, it will get back to the initial value by a heat treatment at 150°C for 1 hour.

## »» CHIP CAPACITOR LAND PATTERN DESIGN RECOMMENDATIONS



Reflow Unit: mm

Size	Z		G		X		Y	
	min	max	min	max	min	max	min	max
0201	0.60	0.90	0.20	0.30	0.25	0.40	0.20	0.30
0402	1.00	1.60	0.40	0.60	0.40	0.60	0.30	0.50
0603	1.70	2.60	0.50	1.00	0.60	1.00	0.60	0.80
0805	2.00	3.80	0.60	1.20	0.90	1.60	0.70	1.30
1206	3.80	5.70	1.80	2.50	1.20	2.00	1.00	1.60
1210	3.80	5.70	1.80	2.50	1.80	3.20	1.00	1.60
1812	4.90	7.50	2.50	3.70	2.30	3.50	1.20	1.90
2220	5.60	9.30	3.20	4.70	3.50	5.00	1.20	2.30
2225	5.60	9.30	3.20	4.70	3.50	6.80	1.20	2.30

Wave Unit: mm

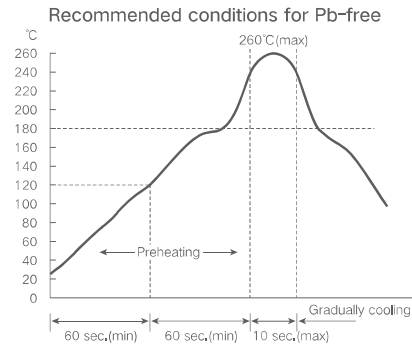
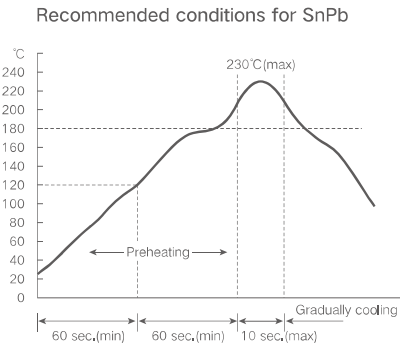
Size	Z		G		X		Y	
	min	max	min	max	min	max	min	max
0603	1.70	2.60	0.50	1.00	0.60	1.00	0.60	0.80
0805	2.60	4.40	1.00	1.40	0.90	1.60	0.70	1.30
1206	3.80	5.70	1.80	2.50	1.20	2.00	1.00	1.60
1210	3.80	5.70	1.80	2.50	1.80	3.20	1.00	1.60

# APPLICATION GUIDE FOR MULTILAYER CERAMIC CAPACITORS

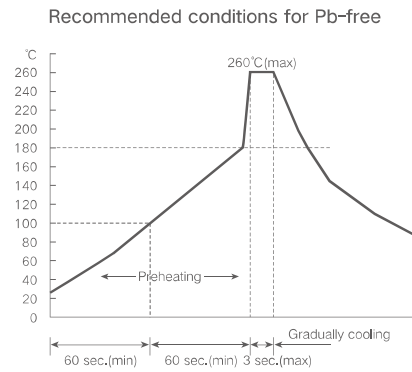
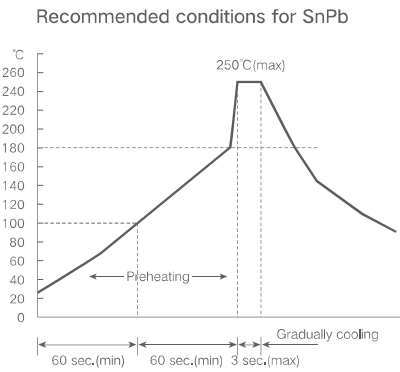
## » SOLDERING

Ceramic chip capacitors are susceptible to thermal shock when exposed to rapid or concentrated heating or rapid cooling. Therefore, the soldering must be conducted with great care so as to prevent malfunction of the components due to excessive thermal shock.

### [ Reflow Soldering ]

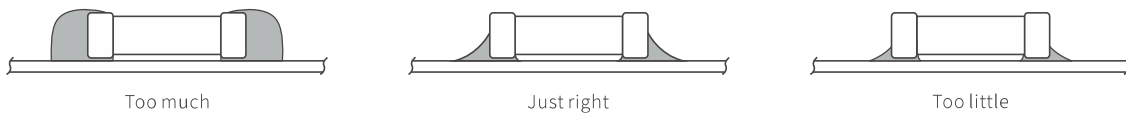


### [ Wave Soldering ]



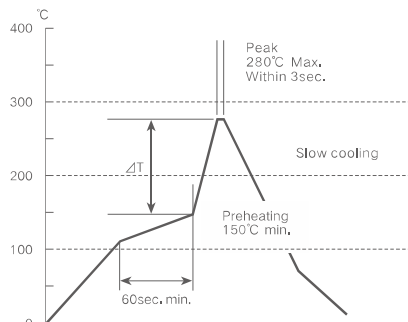
### CAUTION:

If the solder amount is excessive, the risk of cracking is higher during board bending or any other stressful condition. Too little solder amount results in a lack of adhesive strength on the termination, which may result in chips breaking loose from the PCB.



### [ Hand soldering ]

#### Recommended conditions for Hand-soldering



Size	$\Delta T$
1206 or less	$\leq 150^{\circ}\text{C}$
1210 or more	$\leq 130^{\circ}\text{C}$

### CAUTION:

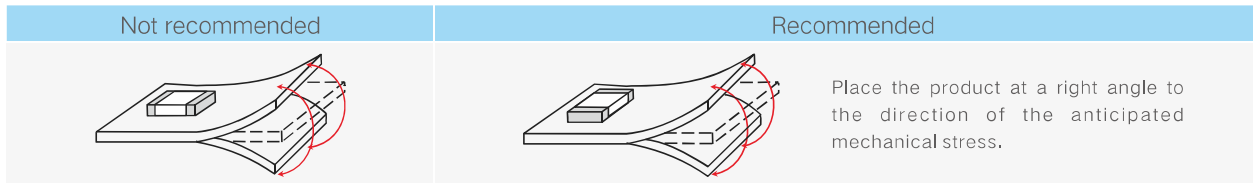
1. Use a maximum tip diameter of 1.0 mm.
2. The soldering iron shall not directly touch capacitors. soldering for 1 times.



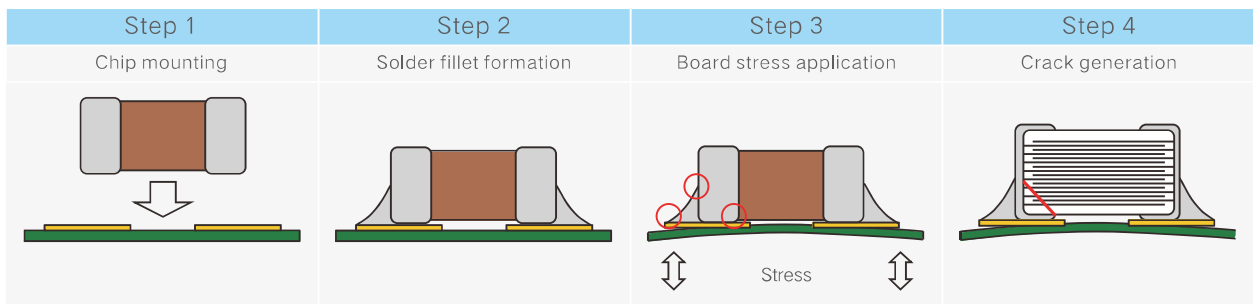
# APPLICATION GUIDE FOR MULTILAYER CERAMIC CAPACITORS

## »» SOLDERING

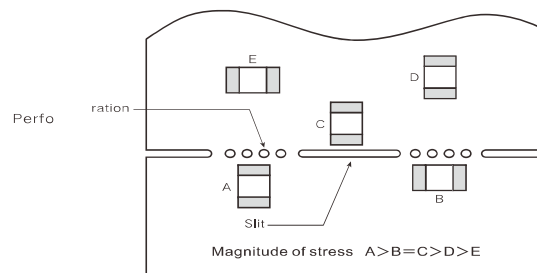
- The following is examples of good and bad capacitor layouts, capacitors shall be located to minimize any possible mechanical stresses from board warp or deflection.



Capacitor was cracked by external mechanical stress such as board distortion and twist applied after mounting.



- The amount of mechanical stresses given will vary depending on capacitor layout. Please refer to the right figure.



- When PCB is split, the amount of mechanical stress on the capacitors can vary according to the method used. The following methods are listed in order from most stressful to least stressful: push-back, slit, V-grooving, and perforation. Thus, please consider the PCB, split methods as well as chip location.

## »» ADJUSTMENT OF MOUNTING MACHINE

When the bottom dead center of a pick-up nozzle is too low, excessive force is imposed on capacitors and causes damages. To avoid this, the following points shall be considerable.

- The bottom dead center of the pick-up nozzle shall be adjusted to the surface level of PCB without the board deflection.
- The pressure of nozzle shall be adjusted between 1 and 3 N static loads.
- To reduce the amount of deflection of the board caused by impact of the pick-up nozzle, supporting pins or back-up pins shall be used on the other side of the PCB. The following diagrams show typical example of good and bad pick-up nozzle placement:

